IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Stephen L. Buchwalter, et al.

Examiner: Khiem D. Nguyen

Serial No: 09/782,494

Art Unit: 2823

Filed: February 13, 2001

Docket: YOR920000745US1 (14029)

For: BILAYER WAFER-LEVEL UNDERFILL

Dated: April 25, 2004

Confirmation No: 9921

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' BRIEF ON APPEAL

1. Real Party in Interest

The real party in interest of the present application is International Business Machines Corporation, the assignee of the entire right, title and interest in the above-identified patent application.

2. Related Appeals and Interferences

No other appeals or interferences are known which directly affect, or will be directly affected by, or have a bearing on, the disposition of the pending appeal.

3. Status of the Claims

The present application was filed on February 13, 2001 with Claims 1-32. In response to a Restriction Requirement imposed in an Office Action dated March 11, 2002, Appellants elected, without traverse, to prosecute Claims 1-22 in a Response dated April 10, 2002. The non-elected claims, i.e. 23-32, were subsequently withdrawn from the case, as being directed to a non-elected invention.

A first Office Action on the merits issued June 19, 2002 to which Appellants filed an Amendment and Response dated September 19, 2002. In this response, Appellants amended Claim 1. A Final Rejection was issued on December 4, 2002, in which the Examiner indicated that Clams 21-22 were allowable subject matter, but maintained the rejections to Claims 1-20. In response to the Final Rejection dated December 4, 2002, Appellants submitted remarks in a Response under 37 C.F.R. §1.116, dated February 4, 2003, in which there were no amendments to the claims. An Advisory Action was issued on February 14, 2003, in which the Examiner maintained the rejections to Claims 1-20. A Request for Continued Examination (RCE) was filed on March 4, 2003. In connection with the RCE, an amendment was submitted, in which Claim 1 was amended for a second time.

In response to an Office Action dated March 31, 2003, Claim 1 was amended for a third time in Appellants' Response dated June 30, 2003. A Final Rejection was issued on September 24, 2003. In response to the Final Rejection dated September 24, 2003, Appellants submitted a Response, under 37 C.F.R. §1.116, dated December 23, 2003, in which Appellants also submitted an unsigned copy of an affidavit under 37 C.F.R. §1.131

indicating Appellants' invention predated a prior art reference. No amendments to the finally rejected claims were submitted with Appellants' Response dated December 23, 2003.

An Advisory Action was issued on January 27, 2004. In response to the Final Rejection (dated September 24, 2003) and the Advisory Action (dated January 27, 2004), Appellants filed a Notice of Appeal on February 24, 2004. Appellants submitted a signed copy of the affidavit, which was originally submitted on December 23, 2003, to the Examiner on April 1, 2004.

Thus, Claims 1-22 are the subject of this appeal; these claims, as they presently stand, are set forth in the Appendix of this Appeal Brief. The status of each of the claims is thus as follows:

Claims 1-20: Finally rejected and on appeal.

Claims 21-22: Allowed.

Claims 23-32: Withdrawn.

4. Status of the Amendment

A Response to the Final Rejection dated September 24, 2003 containing arguments for patentability was filed on December 23, 2003. No amendments to the claims were filed with the December 23, 2003 Response; hence that Response was entered and considered by the Examiner.

5. Summary of Invention

The invention embodied by Claims 1-22, on appeal, relates to a method of forming a microelectronic interconnect structure (depicted in FIGS. 1A-H) containing a bilayer underfill layer comprising the steps of forming a first polymeric material 14 on a surface of a semiconductor wafer 10 having interconnect pads 12 disposed thereon; patterning the first polymeric material 14 to provide openings that expose the interconnect pads 12; forming conductive bump material 18 in the openings; forming a second polymeric material 20 that is partially cured to a B-stage state atop said first polymeric material 14 and conductive bump material 18; dicing said semiconductor wafer 10 into individual chips; and bonding at least one of the individual chips 22 to an external substrate 24, wherein during bonding the conductive bump material 18 penetrates the second polymeric material 20 and contacts a surface of the external substrate 24.

6. Issues on Appeal

I. Do the combined disclosures of U.S. Patent No. 6,228,678 to Gilleo, et al. ("Gilleo, et al.") and U.S. Patent Publication No. 2002/0105092 to Coyle ("Coyle") render Claims 1-20, on appeal, unpatentable under 35 U.S.C. §103(a)?

7. Grouping of the Claims

The Claims involved in Issue I stand and fall together.

8. Arguments for Patentability

I. The combined disclosures of Gilleo, et al. and Coyle do not render Claims 1-20, on appeal, unpatentable under 35 U.S.C. §103(a).

In the Final Rejection dated September 24, 2003, Claims 1-20 were rejected under 35 U.S.C. §103 as allegedly unpatentable over the combination of Gilleo, et al. and Coyle. Appellants respectfully disagree with the Examiner's conclusion that the combination of Gilleo, et al. and Coyle render Appellants' invention unpatentable and submit the following.

To establish a prima facie case of obviousness, under 35 U.S.C. §103, three criteria must be met. First there must be some suggestion or motivation, either in the references themselves or the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references) combined must teach or suggest all of the claimed limitations. Finally, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must be both found in the in the prior art and not based on applicants disclosure. *See Hodosh v. Block Drug Co., Inc.,* 786 F.2d 1136, 1143, 229 USPQ 182, 187 (Fed. Cir. 1986).

Appellants submit that the claims of the present application are not rendered obvious by the applied prior art, since the applied prior art fails to teach each and every element of Appellants' claimed method, as recited in Claim 1, on appeal. The primary reference, Gilleo, et al., as acknowledged by the Examiner, fails to teach or suggest a method for forming a microelectronic interconnect structure comprising the step of *forming a second polymeric material that is partially cured to a B-stage state atop the first polymeric material*

and the conductive bump material. The sole secondary reference cited by the Examiner, Coyle, in the obviousness rejection, does not qualify as prior art and therefore cannot be applied to fulfill the deficiencies of the primary reference. Further, despite failing to qualify as a reference, Coyle fails to teach or suggest a method for forming a microelectronic interconnect structure comprising the step of *forming a second polymeric material that is partially cured to a B-stage state atop the first polymeric material and the conductive bump material.* Finally, there is no motivation to combine the disclosures of Gilleo, et al. with Coyle to produce Appellants' claimed method, as recited in Claim 1, on appeal. The Appellants' remarks are now discussed in greater detail.

a. Appellants' method is not obvious over the disclosure of Gilleo, et al., since Gilleo, et al. fail to teach or suggest each and every aspect of Appellants' claimed method, as recited in Claim 1, on appeal.

Appellants' method is not made obvious by the disclosure of Gilleo, et al., since the applied reference does not teach or suggest Appellants' claimed method. Specifically, Gilleo, et al. do not teach or suggest forming a bilayer underfill, "comprising the steps of forming a first polymeric material on a surface of a semiconductor wafer having interconnect pads disposed thereon; patterning the first polymeric to provide openings that expose the interconnect pads; forming conductive bump material in the openings; *forming a second polymeric material that is partially cured to a B-stage state atop the first polymeric material and the conductive bump* material; dicing the semiconductor wafer into individual chips; and bonding at least one of said individual chips to an external substrate, wherein

during such bonding the conductive bump material penetrates the second polymeric material and contacts a surface of the external substrate", as recited in Claim 1, on appeal. "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art" *In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970).

Gilleo, et al. fail to render Appellants' claimed method unpatentable, under 35 U.S.C. §103(a), since Gilleo, et al. do not teach or suggest "*forming a second polymeric material that is partially cured to a B-stage state atop the first polymeric material and the conductive bump material*", as recited in Claim 1, on appeal. Appellants observe, referring to Page 5 of the Final Rejection dated December 4, 2002, that the Examiner agreed that, "Gilleo fails to teach a partially cured second polymeric material over a first polymeric material and conductive bump material".

Appellants' further submit that Gilleo, et al. fail to teach or suggest partially curing the second polymeric material 14 to a B-stage state. Curing a polymeric material to a B-stage state requires advancing the reaction of a thermosetting polymer to below the gel point to which the material becomes insoluble. The gel point is the point at which cross-linking occurs. B-staging renders thermosetting materials non-tacky since it raises the glass transition temperature of the polymer to above room temperature. Tacky materials are soft at room temperature. In thermoplastics, this is not possible because thermoplastics do not react. Thermoplastics do not cross-link because all the reactions to the polymer backbone have concluded.

Gilleo, et al. do not teach or suggest partially curing the second polymeric layer to a B-stage state. Appellants observe that one embodiment of the Gilleo, et al. disclosure is a

first polymeric layer which includes a thermoplastic resin as the main component and a B-stage thermoset as a lesser component. Although Gilleo, et al. disclose that B-stage thermosets may be present in the first polymeric layer there is no teaching or suggestion of a B-stage thermoset being utilized in the second polymeric layer. Referring to Column 8, line 43-65, the second polymeric layer disclosed in Gilleo, et al. comprises a flux system including epoxy resins. Appellants note, referring to Page 5 of the Final Rejection, dated September 24, 2003, that the Examiner agreed that Gilleo, et al. fail to teach that the second polymeric material is partially cured to a B-stage state, as recited in Claim 1, on appeal.

Additionally, Gilleo, et al. disclose the use of thermoplastic polymers as the main component of the underfill. Specifically, Gilleo, et al. referring to Column 7, lines 29-31, disclose that their method eliminates the problems associated with thermoset underfills by incorporating thermoplastics. Therefore, the Gilleo, et al. disclosure teaches away from Appellants' claimed invention because Gilleo, et al. favor thermoplastics that cannot be cured to a B-stage state.

Therefore, Gilleo, et al. fail to teach or suggest each and every limitation of Appellants' claimed method, since Gilleo, et al. fail to teach or suggest *forming a second polymeric material that is partially cured to a B-stage state atop said first polymeric material and said conductive bump material.*

b. Appellants' method is not obvious, under 35 U.S.C. §103(a), over the combination of Gilleo, et al. and Coyle, since Gilleo, et al. fail to teach or suggest each and every aspect of Appellants' claimed method and Coyle does not qualify as prior art under 35 U.S.C. §102.

Coyle fails to fulfill the deficiencies of the primary reference, Gilleo, et al., and therefore fails to render Appellants' method unpatentable, under 35 U.S.C §103(a), since Coyle does not qualify as a prior art reference, under 35 U.S.C. §102. To establish a prima facie case of obviousness each prior art reference cited must qualify as prior art, under 35 U.S.C. §102. *See Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1568, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). Appellants assert that Coyle is not prior art, under 35 U.S.C. §102, since Appellants' invention was completed in this country prior to the U.S. filing date of the Coyle application.

To evidence Appellants' invention prior to Coyle an unsigned declaration was submitted in Appellants' Response, dated December 23, 2003, which asserted that the secondary reference Coyle is not prior art to the present invention insofar as the present invention was completed in this country before February 2, 2001. A signed copy of this declaration was submitted on April 1, 2004.

Despite the submission of the affidavit under 37 C.F.R. §1.131 predating the Coyle reference, the Examiner maintained that Coyle was prior art in the Advisory Action dated January 27, 2004. It is the Examiner's position that despite the supplied photocopies of the figures and records submitted in the 37 C.F.R. §1.131 affidavit, Appellants failed to provide a satisfactory explanation pertaining to the reduction of practice of Appellants' invention prior to the effective date of the Coyle reference. Appellants respectfully disagree and submit the following.

In a Rule 131 affidavit, the applicant must set forth facts showing completion of the invention in this country prior to the date of the reference. *See In Purdue Pharma L.P. v.*

Boehringer Ingelhiem GmbH, 98 F.Supp2d 362, 55 USPQ2d 1168 (S.D. N.Y. 2000). When alleging that conception or reduction to practice occurred prior to the effective date of the reference, the dates in the oath or declaration may be the actual dates, or if the applicant does not desire to disclose his or her actual date, he or she may merely allege that the acts referred to occurred prior to a specified date. See *Ex part Gasser*, 1880 C.D. 94 (Comm'r Pat. 1880), see also MPEP 715.07. The 37 C.F.R. §1.131 affidavit or declaration must establish possession of the invention or something falling within the claim, in the sense that the claim as a whole reads on the content of the affidavit. *In re Tanczyn,* 347 F.2d 830, 146 USPQ 298 (CCPA 1965). Finally, the PTO requires that the required facts "be shown by evidence in the form of exhibits accompanying the affidavit or declaration." See MPEP 715.07.

Appellants respectfully submit that the evidence submitted with the 1.131 affidavit demonstrates reduction to practice of Appellants' claimed invention in this country prior to the effective date of the Coyle reference. Referring to Page 2 of the §1.131 affidavit, Appellants' have provided exhibits in the form of date redacted invention disclosures (Exhibit Ai) and date redacted internal presentations (Exhibit B) including optical micrographs of the claimed conductive bump material, which penetrates a second polymeric material and contacts the surface of an external substrate. Both Exhibit Ai and Exhibit B where created within the United States at the laboratories of IBM corporation in Yorktown Heights, NY, prior to February 2, 2001, the effective date of Coyle.

Appellants further note that the submitted evidence incorporated within the affidavit establishes possession of the invention, in the sense that the claim as a whole reads on the content of the affidavit. Claim 1 directed to Appellants' method of forming a

microelectronic interconnect structure containing a bilayer underfill layer comprising the steps of:

> (a) forming a first polymeric on a surface of a semiconductor wafer having interconnect pads disposed thereon;
>
> (b) patterning the first polymeric material to provide openings that expose the interconnect pads;
>
> (c) forming conductive bump material in the openings;
>
> (d) forming a second polymeric material that is partially cured to a B-stage state atop the first polymeric material and the conductive bump material;
>
> (e) dicing the semiconductor wafer into individual chips; and
>
> (f) bonding at least one of said individual chips to an external substrate, wherein during bonding the conductive bump material penetrates the second polymeric material and contacts a surface of the external substrate.

The evidence provided within the affidavit as a whole reads on Claim 1, on appeal, and therefore demonstrates completion of Appellants' invention prior to the effective date of Coyle. See *In re Tanczyn*, 347 F.2d 830, 146 USPQ 298 (CCPA 1965). More specifically, Exhibit A(ii), FIG. 1(a) illustrates a silicon wafer with ball limiting metallurgy (BLM) that may function as interconnect pads. FIG. 1(b) depicts applying a first underfill layer, i.e., polymeric, on a surface of a semiconductor wafer, as recited in step (a) of Claim 1. FIG. 1(c) depicts patterning the polymeric material to provide openings in the first underfill layer and exposing the area above the wafer pads, as recited in step (b) of Claim 1. FIG. 2(a) illustrates applying solder, also referred to as conductive bump material, into the openings, as recited in step (c) of Claim 1. Turning now to FIG. 2(b), a second polymeric material is deposited atop the first polymeric material and the conductive bump material, as recited in step (d) of Claim 1. FIG. 3(a) depicts a chip formed by dicing a semiconductor wafer, as

recited in step (e) of Claim 1. FIG. 3(c) depicts bonding at least one of the chips to an external surface, where during bonding the conductive bump material penetrates the second polymeric material and contacts a surface of the external substrate, as recited in step (f) of Claim 1, on appeal.

Further, Exhibit B includes a true photocopy of a transmission electron micrograph of the conductive bump material and bilayer underfill of a microelectronic device formed from the above method, providing actual reduction to practice of the present invention prior the February 2, 2001 filing date of Coyle. More specifically, referring to the micrograph on the slide titled "Cure/Bond Study- Polymide adhesive" a B-staged second polymeric material is depicted as part of the underfill, where bonding and good wetting of the underfill was observed. Therefore, the previously submitted 37 C.F.R. §1.131 affidavit establishes possession of Appellants' claimed invention.

Clearly, the information provided by the previous submitted Declaration, under 37 C.F.R. §1.131, indicates that the present invention was completed by Appellants in the United States prior to the effective filing date of Coyle. Consequently, Coyle is antedated and therefore does not qualify as prior art under 35 U.S.C. §102. Coyle cannot be used as a reference against the claims of the present application.

c. Appellants' method is not obvious over the combination of Gilleo, et al. and Coyle, since Coyle fails to fulfill the deficiencies of Gilleo, et al., as recited in Claim 1, on appeal.

Despite failing to qualify as prior art, Coyle does not alleviate the deficiencies of Gilleo, et al., since Coyle also fails to teach or suggest Appellants' claimed method. Specifically, Coyle does not teach or suggest forming a bilayer underfill, "comprising the steps of forming a first polymeric material on a surface of a semiconductor wafer having interconnect pads disposed thereon; patterning said first polymeric to provide openings that expose said interconnect pads; forming conductive bump material in said openings; *forming a second polymeric material that is partially cured to a B-stage state atop said first polymeric material and said conductive bump* material; dicing said semiconductor wafer into individual chips; and bonding at least one of said individual chips to an external substrate, wherein during such bonding said conductive bump material penetrates said second polymeric material and contacts a surface of said external substrate", as recited in Claim 1, on appeal.

Coyle discloses a method for producing a robust molded chip scale package having a chip with bumped flip chip interconnection to a flexible film substrate including conventional underfill process steps. More specifically, referring to Paragraph 0045 and FIG. 5a, Coyle discloses a conventional underfill method where a plurality of IC chips 50 having bump contacts 51 are aligned to receiving pads on patterned flexible film substrate 52, and the bumps are adhered to the substrate 52. Now referring to FIG. 5b, an underfill material 54 is dispensed under each chip 50, and the polymeric material 54 is partially cured. Referring to Paragraph 0046 and FIG 5c, a plastic encapsulate 58 is then applied over the entire structure.

Appellants submit that the method disclosed in Coyle is substantially removed from Appellants' claimed method in which the first polymeric material (underfill) 14 and the

second polymeric material 20 are applied prior to bonding the IC chip 24. In addition to teaching a substantially different method, Appellants submit that Coyle fails to teach or suggest a second polymeric layer that is partially cured to a B-stage state *atop a first polymeric material and conductive bump material.* It is the Examiner's position that "Coyle discloses forming a second polymeric material 58 that is partially cured to a B-stage state over the first polymeric material 52 and the conductive bump material 51." Appellants disagree and note that reference number 58 denotes an encapsulating material, which is formed atop the IC chips 50 that are bonded to the bump contacts 51 atop the flexible film substrate 52. The encapsulating material 58, referred to by the Examiner as the second polymeric material, is not positioned atop the bump contacts 51 or beneath the IC chip 50. The encapsulating material 58 disclosed in Coyle provides electrical and mechanical protection for the IC chip 50 by enclosing the IC chip 50 in a rigid plastic. *See* Paragraph 0038.

Therefore, because Coyle discloses that the IC chip 50 is positioned between and separates the encapsulating material 58 and the bump contacts 51, Coyle does not teach or suggest forming a second polymeric material that is partially cured to a B-stage state atop the first polymeric material and the conductive bump material, as recited in Claim 1, on appeal.

d. Appellants' method is not obvious over the combination of Gilleo, et al. and Coyle, since there is no motivation to modify the methods disclosed in the referenced prior art to produce Appellants' claimed method, as recited in Claim 1, on appeal.

The §103 rejection also fails because there is no motivation in the applied references which suggests modifying the methods disclosed in Gilleo, et al. and Coyle to include Appellants' claimed method having the process step of forming a second polymeric material that is partially cured to a B-stage state atop the first polymeric material and the conductive bump material, as recited in Claim 1, on appeal. This rejection is thus improper since the prior art does not suggest this drastic modification. The law requires that a prior art reference provide some teaching, suggestion, or motivation to make the modification obvious.

To establish a prima facie case of obviousness, the Examiner must show "some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." *Fine*, 837 F.2d at 1074, 5 USPQ2d at 1598. There is no suggestion to combine, however, if a reference teaches away from its combination with another source. *See id.* at 1075, 5 USPQ2d at 1599. "A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant . . . [or] if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant." *In re Gurley*, 27 F.3d 551, 553, 31 USPQ2d 1130, 1131 (Fed. Cir. 1994). If when combined, the references "would produce a seemingly inoperative device," then they teach away from their combination. *In re Sponnoble,* 405 F.2d 578, 587, 160 USPQ 237, 244 (CCPA 1969); see also *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984) (finding no

suggestion to modify a prior art device where the modification would render the device inoperable for its intended purpose).

Here, there is no motivation provided in the disclosures of the applied prior art references, or otherwise of record, which would lead one skilled in the art to modify the methods of the applied references to include Appellants' claimed sequence of processing steps recited in Claim 1, on appeal. Appellants submit that one of ordinary skill in the art would not be motivated to combine Gilleo, et al. with Coyle, because the applied references teach away from the Examiner's proposed combination. A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore and Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983).

Gilleo, et al. are concerned with reworking during chip mounting process steps and overcoming the disadvantages of thermoset underfills. Gilleo, et al. disclose, referring to Column 7, lines 29-35, that the problems associated with thermoset underfills can be overcome by incorporating a thermoplastic as a main constituent of the of the underfill. Coyle, referring to Paragraph 0010, discloses a conventional underfill process where an objective of the process is to produce a robust molded chip scale package. Coyle further discloses, referring to Paragraph 0036, that underfill materials provide mechanical stability to the device and that in producing a robust molded chip scale package thermosetting underfill materials are preferred. Therefore, since Gilleo, et al. teach that thermosetting underfills should be avoided for the purposes of reworking and Coyle discloses that thermosetting underfills are preferred for increasing the mechanical strength of the chip, the applied references teach away from their combination.

Additionally, one of ordinary skill in the art reading the disclosure of Gilleo, et al. would conclude that incorporating a thermosetting material as a constituent of the of the underfill, as taught by Coyle, changes the principle of operation of the Gilleo, et al. method, since thermosetting materials impair reworking. If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

Therefore, one of ordinary skill in the art would not be motivated to combine the Coyle and Gilleo, et al. references to produce the Appellants' claimed method.

In view of the above remarks, Appellants respectfully submit that Claims 1-20 are patentable subject matter over the combined disclosures of Gilleo, et al. and Coyle.

9. Conclusion

The above arguments establish that all of the claims on appeal are enabled, definite and patentable over the substantive grounds of rejection raised in the Final rejection. Appellants therefore respectfully request that the substantive ground used in rejecting Claims1-20, on appeal, made by the Examiner, be reversed by the Broad of Patent Appeals and Interferences.

Respectfully submitted,

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APPENDIX

10. The claims on appeal for U.S. Application Serial No. 09/782,494, filed March August 31, 2001

1. A method of forming a microelectronic interconnect structure containing a bilayer underfill layer comprising the steps of:

(a) forming a first polymeric on a surface of a semiconductor wafer having interconnect pads disposed thereon;

(b) patterning said first polymeric material to provide openings that expose said interconnect pads;

(c) forming conductive bump material in said openings;

(d) forming a second polymeric material that is partially cured to a B-stage state atop said first polymeric material and said conductive bump material;

(e) dicing said semiconductor wafer into individual chips; and

(f) bonding at least one of said individual chips to an external substrate, wherein during said bonding said conductive bump material penetrates said second polymeric material and contacts a surface of said external substrate.

2. The method of Claim 1 wherein said first polymeric material is formed by a deposition process selected from the group consisting of spin coating, dip coating, brushing, chemical vapor deposition (CVD) plasma-assisted CVD, sputtering, and chemical solution deposition.

3. The method of Claim 2 wherein said deposition process is spin coating.

4. The method of Claim 1 wherein said first polymeric material is a dielectric polymeric material selected from the group consisting of polyimides, polyamides, Si-containing polymers, parylene polymers, polybenzocyclobutane and epoxies.

5. The method of Claim 4 wherein said first polymeric material is an epoxy.

6. The method of Claim 1 wherein said first polymeric material further includes an inorganic filler.

7. The method of Claim 6 wherein said inorganic filler is silica, fumed silica, alumina, titanium dioxide, glass fibers or mixtures thereof.

8. The method of Claim 6 wherein said inorganic filler is present in said first polymeric material in an amount of from about 10 to about 80 wt.%

9. The method of Claim 1 wherein said first polymeric material has a thickness of from about 25 to about 100 microns.

10. The method of Claim 1 wherein said wafer is composed of a semiconducting material and has one or more devices present therein.

11. The method of Claim 1 wherein step (b) includes lithography and etching.

12. The method of Claim 1 wherein said conductive bump material is solder.

13. The method of Claim 1 wherein said conductive bump material is applied to said openings by injection molding, evaporation, plating, or a paste screening process.

14. The method of Claim 1 wherein said second polymeric material is formed by spin coating.

15. The method of Claim 1 wherein said second polymeric material includes a fluxing agent and an adhesive.

16. The method of Claim 1 wherein said second polymeric material is a thermoplastic or thermosetting adhesive.

17. The method of Claim 1 wherein said second polymeric material has a thickness that is thinner than said first polymeric material.

18. The method of Claim 1 wherein said second polymeric material has a thickness of from about 1 to about 10 microns.

19. The method of Claim 1 wherein said bonding step occurs a temperature of from about 180° to about 260°C for a time period of from about 1 to about 10 minutes.

20. The method of Claim 1 wherein said external substrate is a laminate substrate, a chip carrier, a circuit card or a circuit board, each having interconnect pads formed thereon.

21. A method of forming a microelectronic interconnect structure containing a bilayer underfill layer comprising the steps of:

(a) forming a first polymeric material on a surface of a semiconductor wafer having conductive bump material disposed on portions thereof;

(b) removing a portion of said first polymeric material so as to expose top surfaces of said conductive bump material;

(c) forming a second polymeric material on said first polymeric material and said exposed top surfaces of said conductive bump material;

(d) dicing said semiconductor wafer into individual chips; and

(e) bonding at least one of said individual chips to an external substrate, wherein during said bonding said conductive bump material penetrates said second polymeric material and contacts a surface of said external substrate.

22. The method of Claim 21 wherein step (b) is carried out by polishing or etching.

IFW 2823 AF

TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.: YOR920000745US1

In Re Application Of: **Stephen L. Buchwalter, et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
09/782,494	February 13, 2001	Khiem D. Nguyen	2823

Invention: **BILAYER WAFER-LEVEL UNDERFILL**

Confirmation No: 9921

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on

The fee for filing this Appeal Brief is: **$330.00**

☐ A check in the amount of the fee is enclosed.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **50-0510/IBM**

Signature

Dated: **April 26, 2004**

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I certify that this document and fee is being deposited on **April 26, 2004** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature of Person Mailing Correspondence

Leslie S. Szivos

Typed or Printed Name of Person Mailing Correspondence

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